



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named
Inventor : Judy M. Gehman et al.

Appln. No. : 10/816,213

Filed : April 1, 2004

For : SYSTEM AND METHOD FOR
IMPLEMENTING MULTIPLE
INSTANTIATED CONFIGURABLE
PERIPHERALS IN A CIRCUIT
DESIGN

Docket No.: 03-1002/L13.12-0246

Group Art Unit:
Examiner:

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I HEREBY CERTIFY THAT THIS PAPER IS BEING
SENT BY U.S. MAIL, FIRST CLASS, TO THE
COMMISSIONER FOR PATENTS, P.O. BOX 1450,
ALEXANDRIA, VA 22313-1450, THIS

19 DAY OF July, 20 04.
D. J. B.
PATENT ATTORNEY

Sir:

The patents or publications listed on the enclosed PTO Form-1449 are submitted pursuant to 37 C.F.R. § 1.97. Copies of other related art cited are enclosed.

TIME OF FILING

The information disclosure statement is being filed:

1. X with the application or within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever event occurs last. In accordance with 37 C.F.R. § 1.97(b), no statement or fee is required.
2. _____ after the time period specified in paragraph 1 above, but before the mailing date of a final action under 37 C.F.R. § 1.113 or notice of allowance under 37 C.F.R. § 1.311. Therefore, in accordance with 37 C.F.R. § 1.97(c), submitted herewith is:

(check either A or B below)

- A. ☐ a statement as specified in 37 C.F.R. § 1.97(e).
- B. ☐ the fee set forth in 37 C.F.R. § 1.17(p) for submission of an information disclosure statement under 37 C.F.R. § 1.97(c).
3. ☐ after the mailing date of either a final action under 37 C.F.R. § 1.113 or a notice of allowance under 37 C.F.R. § 1.311, whichever occurs first, but before payment of the issue fee. Therefore, Applicant petitions for consideration and submits herewith:
- A. a statement as specified in 37 C.F.R. § 1.97(e);
- B. the petition fee set forth in 37 C.F.R. § 1.17(p).

STATEMENT

(only used if No. 2(A) or No. 3 above is checked)

The person(s) signing below certify

(check appropriate paragraph)

☐ that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. 37 C.F.R. § 1.97(e)(1).

OR

☐ that no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement. 37 C.F.R. § 1.97(e)(2).

METHOD OF PAYMENT

☒ No fee is required.

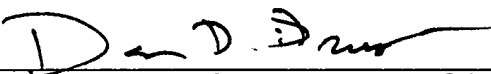
____ Attached is a check in the amount of \$ ____.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123. A duplicate copy of this communication is enclosed.

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

By:



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DDB/RMR/rkp



FORM PTO-1449	Atty. Docket No.: 03-1002/L13.12-0246	Appl. No.: 10/816,213
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	First Named Inventor:	
	Judy M. Gehman et al.	
	Filing Date	Group Art:
	April 1, 2004	

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
AA	6,574,778	06/2003	Chang et al.	716	1	
AB	6,578,174	06/2003	Zizzo	716	1	
AC	6,536,028	03/2003	Katsioulas et al.	716	17	
AD	6,530,074	10/2002	Katsioulas et al.	716	17	
AE	6,366,874	04/2002	Lee et al.	703	14	
AF	6,334,207	12/2001	Joly et al.	716	17	

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub Class	Translation Yes No
AG						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AH	Sutherland, S.; "The IEEE Verilog 1364-2001 Standard What's New, and Why You Need It," 9th Annual International HDL Conference and Exhibition, March 2000. Pp. 1-8.
AI	Cummings, C.; "Verilog-2001 Behavioral and Synthesis Enhancements," Revised April 2002, pp. 1-23.
AJ	Cummings, C.; "New Verilog-2001 Techniques for Creating Parameterized Models (or Down with 'define and Death of a defparam!) HDLCON 2002, pp. 1-10.
AK	Wu, Y.; and MacDonald, P.; "Testing ASICs with Multiple Identical Cores," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, no. 3, March 2003, pp. 327-336.
AJ	Miodrag Potkonjak et al. "Behavioral Synthesis of Area-Efficient Testable Designs Using Interaction Between Hardware Sharing and Partial Scan," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 9, September 1995, pp. 1141-1154.
AL	Chih-Chang Lin et al. "Test-Point Insertion: Scan Paths Through Functional Logic," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 17, no. 9, September 1998, pp. 838-851.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



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AM						
AN						
AO						
AP						
AQ						
AR						

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub Class	Translation Yes No
AS						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AT	Claus Schneider et al. "Modular Metrology Tools for Productivity Enhancement in Wafer Fabs," IEEE International Symposium on Semiconductor Manufacturing, Conference Proceedings, 1997. Oct. 6-8, 1997. Pp. B21-24.
AU	Tianhao Zhang et al. "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Codesign Principles," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 21, no. 8, Aug. 2002, pp. 987-995.
AV	Ryota Kasai et al. "An Integrated Modular and Standard Cell VLSI Design Approach," IEEE Journal of Solid-State Circuits, vol. SC-20, no. 1, Feb. 1985 pp. 407-412.
AW	Jeff Vanderlip. "LSI Logic Physical RTL Optimization (LSI PRO)," LSI Logic Corporation, Oct. 31, 2002. Pp. 1-7.
AX	

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